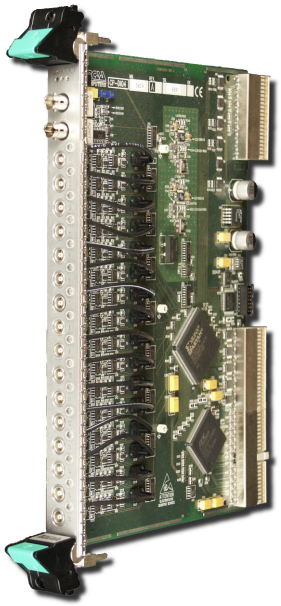
CP-DIO4-5024 Timing generator

NEW

Features



- General purpose digital I/O module with 8 configurable timing channels.
- Optical link input and output for timing highway.
- Timing highway encoder, decoder and recorder.
- 16 digital I/O channels and 8 PXI channels.
- Timers/counters configurable up to 64 bit.
- High accuracy and low jitter clock generation.
- I/O channels available at front or rear side.
- Front panel outputs are short circuit protected and capable of driving 50 Ohm loads.
- Tri-colour status LED per I/O channel.
- Functionality is highly configurable.
- I/O channels and PXI channels are software connectable through a connection matrix.
- LEMO 00 connectors at the front panel.
- Rear side I/O for use with transition modules.
- 6U, single slot CompactPCI form factor.
- 33 MHz, 32 bit PICMG 2.0 R3.0 compatible.

Description

The DIO4 is a general purpose, 16 channel, digital I/O module with 8 flexible assignable timing channels in a 6U high CompactPCI form factor. The 16 I/O channels can be connected via the front panel or the rear side.

The timing channels can be assigned to any of the 16 front or rear side I/Os or to any of the PXI trigger signals. They are synchronized to an external or internal clock. For example the onboard highly accurate and low jitter PLL can be used to increase the Timing Highway clock (1MHz) up to the 10MHz timing channel clock.

Besides functioning as a clock and/or trigger generator the timing channels of the DIO4 can also be used as 32 bit counters. For example, it is possible to count the amount of events or generate a signal after an amount of events. The timing channel counter functionality can be cascaded to create 64 bit counters.

The DIO4 is also capable of providing Timing Highway (Princeton TFTR compatible) encoder, decoder and/or recorder functionality via its front panel optical interface. This Timing Highway is a commonly used timing interface in the plasma physics and fusion research world.

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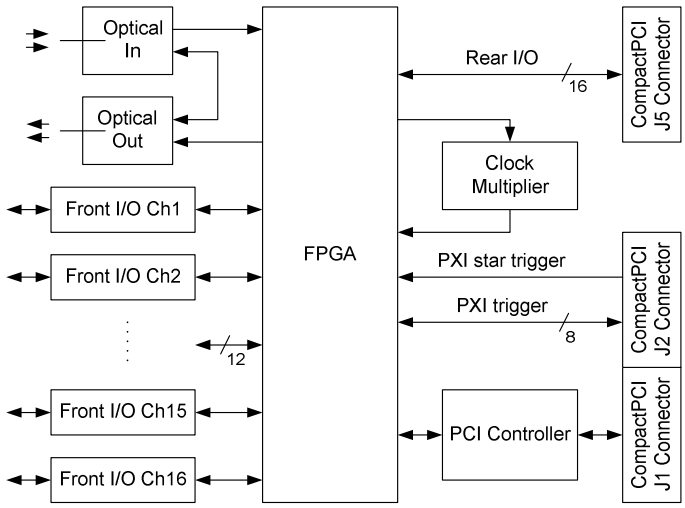
The I/O buffer circuits have built in protection. When the I/O circuit is set to be an output, the input is read back and compared to the driven level. When these are not equal the output is disabled and an error is indicated through a front panel LED, a status bit and/or an interrupt. This error detection is therefore capable of detecting short circuits, driver collisions and severe signal distortions in almost all cases.

Block diagram of DIO4



Connection matrix

From \ To	Register	Front/Rear Out ch. 1 to 16	PXI trigger 0 to 7	Event Encoder ch. 1 to 16	Trigger Timing ch. 1 to 8	Gate Timing ch. 1 to 8	Start Timing ch. 1 to 8	Stop Timing ch. 1 to 8
Register	Via I/O	✓	✓					
Front/Rear In ch. 1 to 16	✓	✓	✓	✓	✓	✓	✓	✓
PXI trigger 0 to 7	✓	✓		✓	✓	✓	✓	✓
PXI star trigger				✓	✓	✓	✓	✓
Event Decoder ch. 1 to 16					✓		✓	✓
Timing Ch. Out ch. 1 to 8	✓	✓	✓	✓	✓	✓	✓	✓

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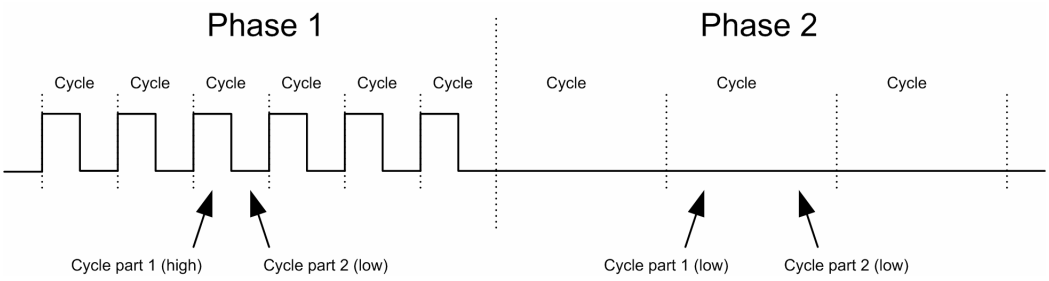
Timing channel

The 8 timing channels are clock and/or trigger signal generators and general purpose digital counters running synchronized to an internal or external clock. The outputs of these timing channels, can be assigned to one or more digital I/Os or PXI trigger signals. They can however also be used directly to trigger or gate other timing channels.

A timing channel has a two phase configuration and a phase itself consists of two parts. The duration of these parts is controlled by separate counters. The output signal can be a continuous low or high DC level, an alternating periodic signal like a clock or a single pulse. This all depends on the configuration of the two cycle part counters.

It is possible to generate two different signals per timing channel since there are two phases. For example the timing channel can be configured to output a clock signal of 200kHz during Phase 1 and a continuous low level during Phase 2. This can be seen in the example below.

Example



The change from one phase to the next can be controlled using different triggers, which can be selected per timing channel. Triggers like: software trigger, front/rear I/O and PXI trigger, the PXI star trigger and a timing channel output are available. A timing event (using an event channel), received via the optical input (Timing Highway) can also be used as a trigger for the timing channel.

The timing channels can be gated. This gate can be a software gate, a front/rear I/O and PXI trigger signal, the PXI star trigger signal or a timing channel output.

Timing Highway

The Timing Highway is an optically interface with bi-phase encoded (Manchester encoded) timing events compatible with the TFTR system at Princeton. The Timing Highway can be used to send or receive up to 127 different timing events. These events can be used to start, stop or trigger the timing channels.

Applications for this module include:

- complex timing generation
- trigger generation
- register based digital I/O
- etc.

The plug and play functionality (not hot swap) provides easy setup and use. The module includes software drivers for Linux.

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Technical Specifications

FRONT PANEL I/O

- Number of frontpanel I/O's : 16
- Connector : 16 x LEMO 00 at front side. Type EPL.OO.250.NTN
- Input type : TTL with hysteresis
- High-level input voltage (min) : 2 V
- Low-level input voltage (max) : 0.8 V
- Input voltage range : -2 V (clamped at -0.3 V) to 7 V
- Input threshold level : 1.4 V with 0.4 V hysteresis
- Input impedance : > 3 kOhm
- Line termination : 50 Ohm, software selectable
- Input frequency (max) : 10 MHz
- Input pulse width (min) : 50 ns
- Output type : TTL, short circuit protected, 50 Ohm drive capability
- High-level output voltage (min) : 4.8 V (no load)
  : 2.4 V (50 Ohm load)
- Low level output voltage (max) : 0.4 V
- Output current : 50 mA (50 Ohm load)
- Output short-circuit current : 140 mA (max)
- Short-circuit duration : Continuous

REAR SIDE I/O

- Number of rear side I/O's : 16
- Connector : CompactPCI, J5
- Input type : TTL
- High-level input voltage (min) : 2 V
- Low-level input voltage (max) : 0.8 V
- Input voltage range : -0.5 V to 5.5 V
- Input frequency (max) : 10 MHz
- Input pulse width (min) : 50 ns
- Output type : Open collector with 1 kOhm pull-up to +5 V.
- High-level output voltage (min) : 4.8 V (no load)
- Low level output voltage (max) : 0.4 V

PXI I/O

- Number of PXI I/O's : 8 I/O's and 1 input only.
- PXI inputs : PXI-TRIG[0]….[7] and PXI_STAR
- PXI outputs : PXI-TRIG[0]….[7],
  PXI_TRIG[7] is a high frequency output
- Input frequency (max) : 40 MHz (PXI_TRIG[7])
  : 10 MHz (PXI_TRIG[0]….[6] and PXI_STAR)

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TIMING CHANNEL

- Clock source : internal or external through front, rear, PXI or optical interface
- Output frequency (max) : 5 MHz
- Counter input frequency (max) : 5 MHz
- Jitter (typ) : < 8 ps (rms) @ 5 MHz generated signal
  : < 13 ps (rms) @ 200 kHz generated signal
  : < 40 ps (rms) @ 1 kHz generated signal

OPTICAL I/O (Timing Highway)

- Connectors : ST style
- Receiver : HFBR2416
- Transmitter : HFBR1414
- Applicable fiber cable : 62.5/125 µm multimode glass
- Power : The power for the optical link can be connected in a redundant way through J5 by an external power supply or through the CompactPCI 5 V.

COMPACTPCI INTERACE

- Version : PICMG 2.0 R3.0
- Bus width : 32 bits
- Clock : 33 MHz
- Configuration : Target (Slave)
- Signal level : 5 V and 3 V
- Interrupt : INTA#
- Connector : J1 only
- Hot swap : No
- Geographical addressing : No

MECHANICAL

- Height : 6U
- Width : 1 slot

ENVIRONMENTAL CONDITIONS

- Max. operating relative humidity : 90 %, no condensation.
- Operating temperature : 15 – 40 ℃

SOFTWARE DRIVER

- Operating system : Linux, others on request

WARRANTY : 1 year

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